

54F/74F219

64-Bit Random Access Memory with TRI-STATE® Outputs

General Description

The 'F219 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are TRI-STATE and are in the high-impedance state whenever the Chip Select (CS) input is HIGH. The outputs are active only in the Read mode. This device is similar to the 'F189 but features non-inverting, rather than inverting, data outputs.

Features

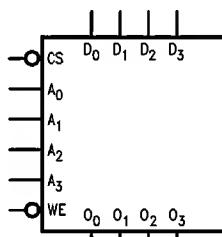
- TRI-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing
- Available in SOIC (300 mil only)

Commercial	Military	Package Number	Package Description
74F219PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F219DL (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F219SC (Note 1)		M16B	16-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F219SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F219FL (Note 2)	W16A	16-Lead Cerpack
	54F219LL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DLQB, FLQB and LLQB.

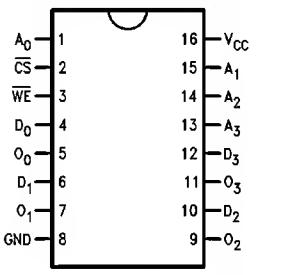
Logic Symbol



TL/F/9500-1

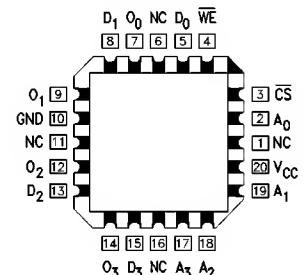
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9500-2

Pin Assignment for LCC



TL/F/9500-3

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Unit Loading/Fan Out

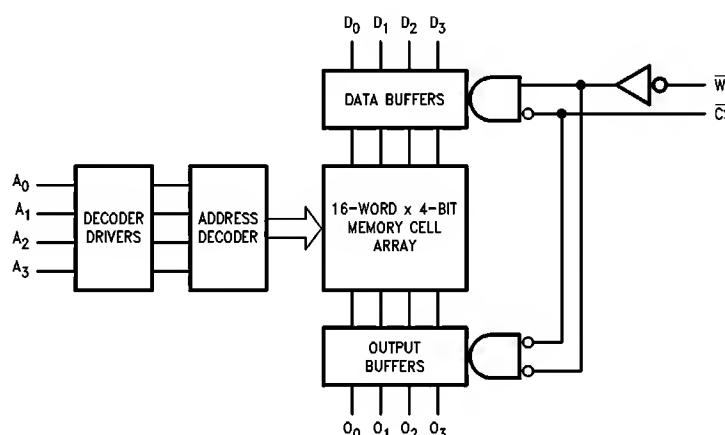
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_3	Address Inputs	1.0/1.0	$20 \mu A/-0.6 \text{ mA}$
\overline{CS}	Chip Select Input (Active LOW)	1.0/2.0	$20 \mu A/-1.2 \text{ mA}$
\overline{WE}	Write Enable Input (Active LOW)	1.0/1.0	$20 \mu A/-0.6 \text{ mA}$
D_0-D_3	Data Inputs	1.0/1.0	$20 \mu A/-0.6 \text{ mA}$
O_0-O_3	TRI-STATE Data Outputs	150/40 (33.3)	$-3 \text{ mA}/24 \text{ mA} (20 \text{ mA})$

Function Table

Inputs		Operation	Condition of Outputs
\overline{CS}	\overline{WE}		
L	L	Write	High Impedance
L	H	Read	True Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



TL/F/9500-4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +100°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage		0.8		V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage		−1.2		V	Min	$I_{IN} = -18\text{ mA}$
V_{OH}	Output HIGH Voltage	54F 10% V_{CC} 54F 10% V_{CC} 74F 10% V_{CC} 74F 10% V_{CC} 74F 5% V_{CC} 74F 5% V_{CC}	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	$I_{OH} = -1\text{ mA}$ $I_{OH} = -3\text{ mA}$ $I_{OH} = -1\text{ mA}$ $I_{OH} = -3\text{ mA}$ $I_{OH} = -1\text{ mA}$ $I_{OH} = -3\text{ mA}$
V_{OL}	Output LOW Voltage	54F 10% V_{CC} 74F 10% V_{CC}		0.5 0.5			$I_{OL} = 20\text{ mA}$ $I_{OL} = 24\text{ mA}$
I_{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	$V_{IN} = 2.7\text{ V}$
I_{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	$V_{IN} = 7.0\text{ V}$
I_{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	74F	4.75		V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
I_{IL}	Input LOW Current			−0.6 −1.2	mA	Max	$V_{IN} = 0.5\text{ V (A}_n, \text{WE, D}_n)$ $V_{IN} = 0.5\text{ V (CS)}$
I_{OZH}	Output Leakage Current			50	μA	Max	$V_{OUT} = 2.7\text{ V}$
I_{OZL}	Output Leakage Current			−50	μA	Max	$V_{OUT} = 0.5\text{ V}$
I_{OS}	Output Short-Circuit Current		−60	−150	mA	Max	$V_{OUT} = 0\text{ V}$
I_{zz}	Bus Drainage Test			500	μA	0.0V	$V_{OUT} = 5.25\text{ V}$
I_{CC}	Power Supply Current		37	55	mA	Max	

AC Electrical Characteristics

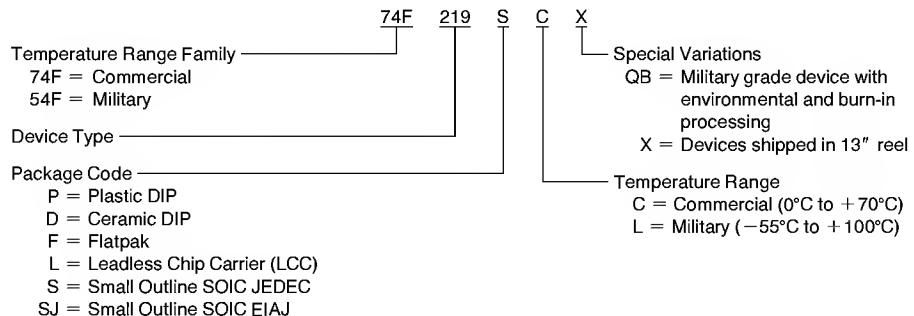
Symbol	Parameter	74F			54F		74F		Units	
		$T_A = +25^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$			$T_A = +100^\circ C$ $V_{CC} = Mil$ $C_L = 50 pF$		$T_A, V_{CC} = Com$ $C_L = 50 pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Access Time, HIGH or LOW A_n to O_n	10.0	18.5	26.0	9.0	32.0	10.0	27.0	ns	
t_{PHL}		8.0	13.5	19.0	8.0	23.0	8.0	20.0		
t_{PZH}	Access Time, HIGH or LOW \overline{CS} to O_n	3.5	6.0	8.5	3.5	10.5	3.5	9.5	ns	
t_{PZL}		5.0	9.0	13.0	5.0	15.0	5.0	14.0		
t_{PHZ}	Disable Time, HIGH or LOW \overline{CS} to O_n	2.0	4.0	6.0	2.0	8.0	2.0	7.0	ns	
t_{PLZ}		3.0	5.5	8.0	2.5	10.0	3.0	9.0		
t_{PZH}	Write Recovery Time HIGH or LOW, WE to O_n	6.5	20.0	28.0	6.5	37.5	6.5	29.0	ns	
t_{PZL}		6.5	11.0	15.5	6.5	17.5	6.5	16.5		
t_{PHZ}	Disable Time, HIGH or LOW \overline{WE} to O_n	4.0	7.0	10.0	3.5	12.0	4.0	11.0	ns	
t_{PLZ}		5.0	9.0	13.0	5.0	15.0	5.0	14.0		

AC Operating Requirements

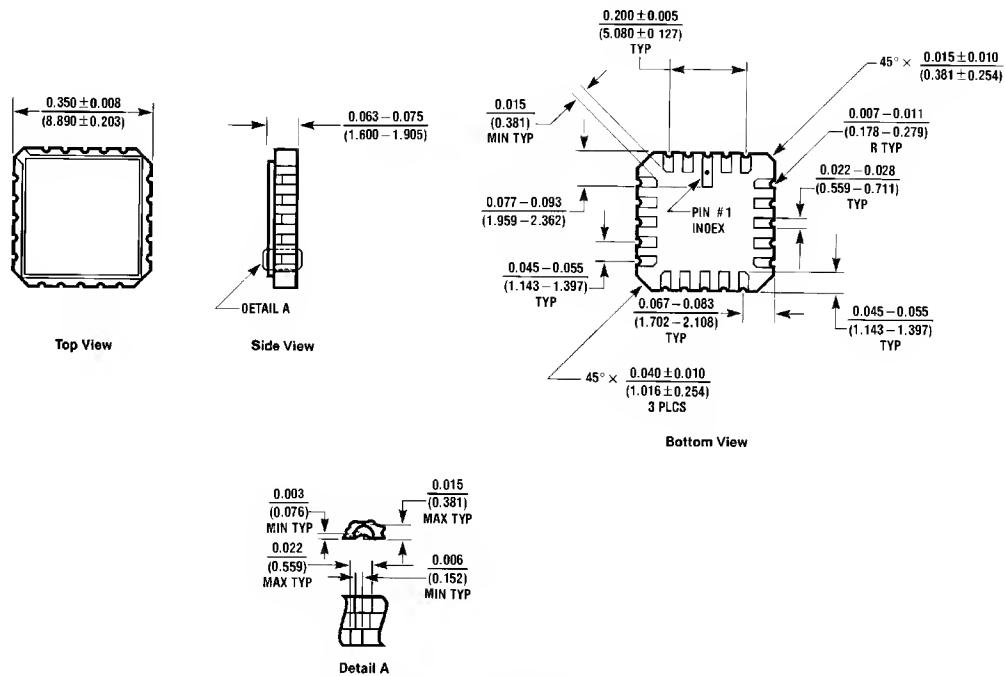
Symbol	Parameter	74F		54F		74F		Units	
		$T_A = +25^\circ C$ $V_{CC} = +5.0V$		$T_A = +100^\circ C$ $V_{CC} = Mil$		$T_A, V_{CC} = Com$			
		Min	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW A_n to \overline{WE}	0		0		0		ns	
$t_s(L)$		0		0		0			
$t_h(H)$	Hold Time, HIGH or LOW A_n to \overline{WE}	2.0		2.0		2.0		ns	
$t_h(L)$		2.0		2.0		2.0			
$t_s(H)$	Setup Time, HIGH or LOW D_n to \overline{WE}	10.0		11.0		10.0		ns	
$t_s(L)$		10.0		11.0		10.0			
$t_h(H)$	Hold Time, HIGH or LOW D_n to \overline{WE}	0		2.0		0		ns	
$t_h(L)$		0		2.0		0			
$t_s(L)$	Setup Time, LOW \overline{CS} to \overline{WE}	0		0		0		ns	
$t_h(L)$	Hold Time, LOW \overline{CS} to \overline{WE}	6.0		7.5		6.0			
$t_w(L)$	\overline{WE} Pulse Width, LOW	6.0		15.0		6.0		ns	

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



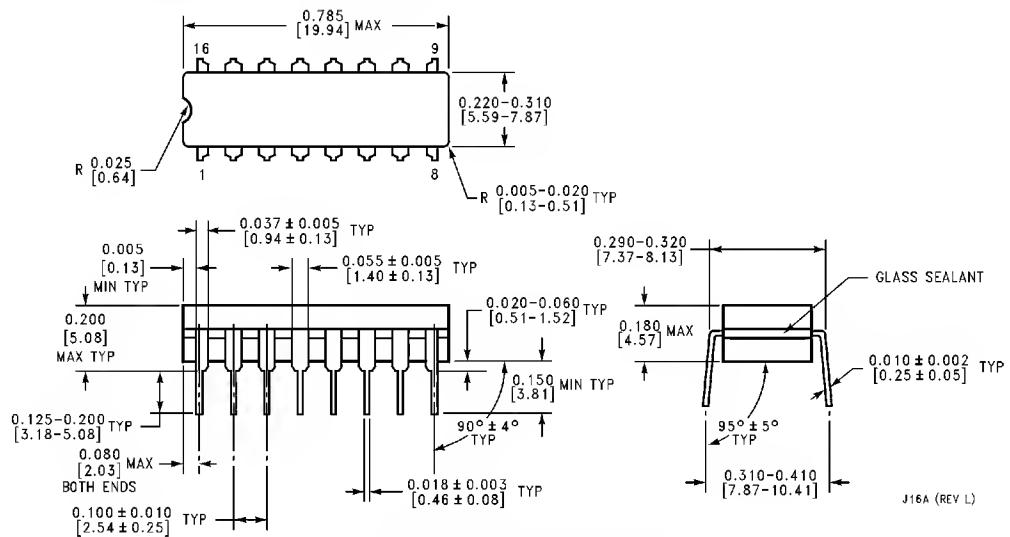
Physical Dimensions inches (millimeters)



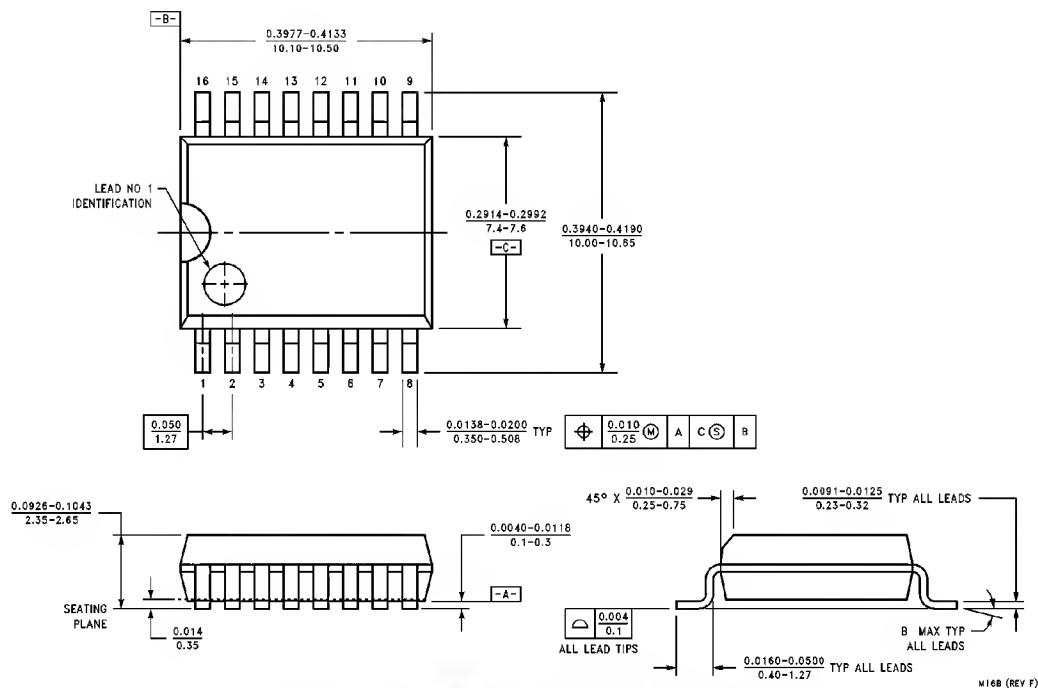
20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

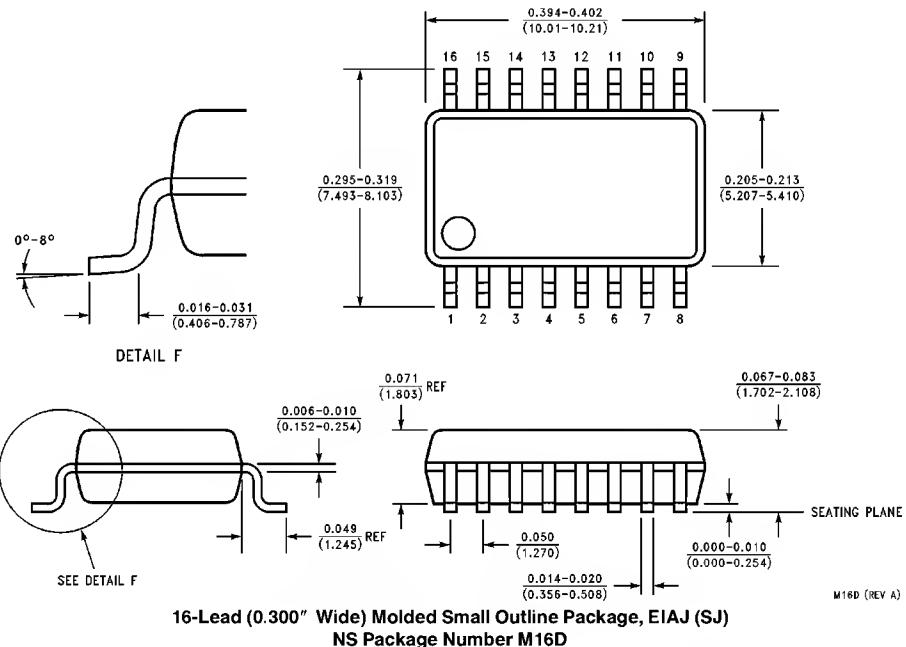


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

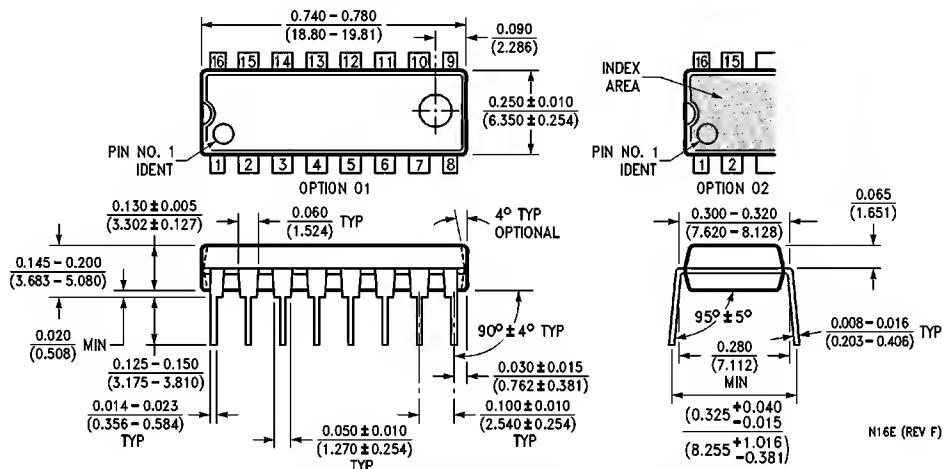


16-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16B

Physical Dimensions inches (millimeters) (Continued)

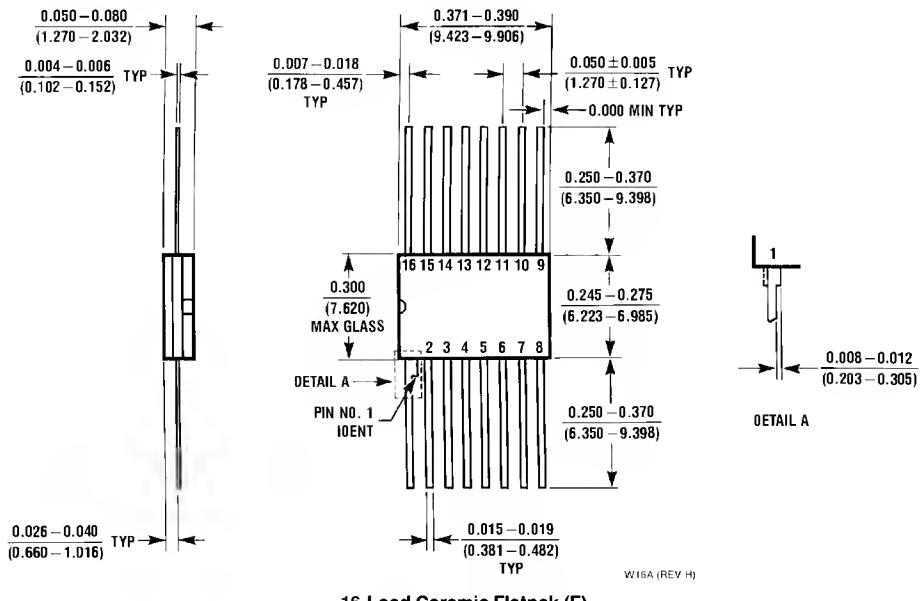


16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



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